ABSTRACT OF THE DISCLOSURE

A bus hold circuit of CMOS components that draws no DC current and is over voltage tolerant is described. No leakage current is drawn from the input when the input voltage is greater than the bus hold circuit supply voltage. A feedback inverter is used to latch the Vin logic in the bus hold circuit. When Vin is low, it turns on a first switch that drives the gate of a PMOS switch low turning it on. The PMOS switch connects the power connection of the feedback inverter to Vcc. The gate remains low, keeping the PMOS switch turned on as Vin increases. The first switch is turned off, but the gate of the PMOS switch remains low, until Vin exceeds Vcc. At that point, a comparator drives the gate of the PMOS to Vin shutting the PMOS switch off. An arbiter circuit selects the higher of Vcc and Vin to bias the N-well of the PMOS switch and other PMOS components in the comparator and arbiter circuit. This biasing ensures that the N-wells are never forward biased, thereby preventing leakage from the Vin.